Amendments to the Specification:

Please amend paragraph [0011]] on page 8 as follows:

[0011] Memory device 190 is a DRAM memory device with an interface made up of control logic 191 and data buffer 197 configured to be interoperable with memory bus. In some embodiments, memory device 190 is a single integrated circuit/ In other embodiments, memory device 190 is made up of multiple integrated circuits of a removable memory module, such as a SIMM (single inline memory module), SIPP (single inline pin package), DIMM (dual inline memory module), etc. It is contemplated that memory device 190 may provide an indication that is readable by another device via memory bus 180 to which memory device 190 is coupled of the ability of the control logic 191 of the memory device 190 to both open a specific row and close a different row in response to receipt of a row activate command to open a specific row.